USB-1604HS-2AO

Specifications

Revision 1.0, March, 2009

Specifications

All specifications are subject to change without notice.

Typical for 25 °C unless otherwise specified.

All signal names refer to 68 pin SCSI connector, unless otherwise specified.

Analog input

Table 1. Analog input specifications

Parameter	Conditions	Specification
A/D converter type		16-bit successive approximation type
Number of AI channels		4 SE simultaneous
Input configuration		Single-ended
Sampling method		Simultaneous; individual A/D per channel
Input ranges		±10 V, ±2.5 V, ±500 mV
Absolute maximum input voltage		*±30 V maximum (power on)* *±20 V maximum (power off)*
Input impedance		10 MΩ (typical, power on)
Input bias current		< 2 µA
Input bandwidth (-3 dB)		3 MHz, typical
Crosstalk	Remaining inputs grounded	100 dB (at 100 kHz)
Pacer sources		▪ Onboard A/D clock or external digital source (XAPCR or EXT CLK BNC) ▪ External pacing (XAPCR or EXT CLK BNC) See Table 12 for additional information.
Trigger sources and modes		See Table 11
Sampling rate		0.01 S/s to 1.33 MS/s each channel, software programmable
Clock sources		Internal, software programmable or external pacing
Resolution		16-bits
INL (integral non-linearity)		±2.0 LSB
DNL (differential non-linearity)		±1.0 LSB

Table 2. Calibrated accuracy

Range	Accuracy
±10 V	±1 mV
±2.5 V	±0.5 mV
±500 mV	±0.15 mV

Table 3. Noise performance, note 1

Range	Typical counts	LSB rms
±10 V	8	1.3
±2.5 V	11	1.6
±500 mV	17	2.5

Note 1: Noise distribution is determined by gathering 50,000 samples with inputs tied to ground at the BNC connectors. Samples are gathered at the maximum specified rate.

Table 4. SINAD (signal to noise and distortion) performance, note 2

Range	Typical SINAD, dB
±10 V	84
±2.5 V	82
±500 mV	77

Note 2: Calibrated and measured with a 10 kHz signal at 0.95 FSR, at the maximum sampling rate.

Table 5. ENOB (effective number of bits) performance, note 3

Range	Typical ENOB, Bits
±10 V	14
±2.5 V	13
±500 mV	13

Note 3: Calibrated and measured with a 10 kHz signal at 0.95 FSR, at the maximum sampling rate.

Table 6. SFDR (spurious-free dynamic range) performance, note 4

Range	Typical SFDR, dB
±10 V	95
±2.5 V	95
±500 mV	95

Note 4: SFDR is measured at the maximum sampling rate.

Analog output

Table 7. Analog output specifications

Parameter	Conditions	Specification
Number of channels		Two independent
Resolution		16-bits
Output range		±10 V
Throughput	Two channel	1 MS/s each channel
Pacer sources		▪ Internal pacing ▪ External pacing ▪ Pacing slaved to analog input pacing See Table 12 for additional information.
Monotonicity		16-bits
Glitch energy		< 12 nV/s
Current output		±5 mA maximum
Output coupling		DC
Power up state		DACs clear to midscale, (0 V, ±20 mV)
Output noise		3 mV rms maximum
Settling time (to .01%FS)	10 V output step, (R_L=5 kΩ, C_L=200 pf)	5 µS
Slew rate		10 V/µs
Gain error		±0.01% of FSR
Zero error		±0.0045 V maximum
INL		< 2 LSBs
DNL		< 1 LSB
Offset error drift		±10 ppm/°C
Gain error drift		±10 ppm/°C

Analog input calibration

Table 8. Analog input calibration specifications

Parameter	Specification
Recommended warm-up time	15 minutes minimum
Calibration methods	Software system calibration and self-calibration
Self-calibration	yes
System calibration interval	1 year
System calibration references	+8.192 V, +2.048 V, +0.4096 V ±5 mV. Actual measured values stored in EEPROM
	Tempco: 5 ppm/°C maximum
	Long term stability: 30 ppm/1000 h

Digital inputs

Table 9. Digital input specifications

Parameter	Specification
Number	16 inputs (DIN0-DIN15)
Digital type	3.3V CMOS (5V tolerant)
Digital input transfer rate (H/W-paced)	Up to 8 MHz — DIO-only operation 1.33 MHz — if configured for AI operations
Input high voltage	2.0 V minimum, 5.5 V maximum
Input low voltage	0.8 V maximum, 0 V minimum
Absolute maximum input voltage	15 V (power-on and power-off conditions)
DIN pacing	On-board or external clock (XAPCR)
Pacer sources	▪ Internal pacer clock or external digital source (XAPCR or EXT CLK BNC). ▪ External pacer clock (XAPCR or EXT CLK BNC) See Table 12 for additional information.
DIN trigger modes and sources	See Table 11
Input pull-ups	100 kΩ (consult factory for alternative options)
Latency, software paced	115 ms, typical (system dependant)

Digital outputs

Table 10. Digital output specifications

Parameter	Specification
Number	16 outputs (DOUT0-DOUT15)
Digital output rate	8 MHz maximum if no analog outputs are enabled, (1 MHz maximum if analog outputs are enabled)
Digital type	3.3 V CMOS
Output high voltage (IOH = –2.5 mA)	2.4 V minimum, 3.4 V maximum
Output low voltage (IOL = 2.5 mA)	0.4 V maximum, 0 V minimum
Output current	2.5 mA maximum per pin
DOUT pacing	On-board or external clock (XDPCR)
Pacer sources	▪ Internal pacing ▪ External pacing ▪ Pacing slaved to analog input pacing See table 12 for additional information.
Outputs at power on and reset	Low
Latency, software paced	115 ms, typical (system dependant)

Trigger sources

Table 11. External trigger specifications

Parameter	Specification
Available trigger sources	▪ Analog input hardware ▪ Analog software trigger ▪ External digital input ▪ Digital pattern ▪ Counter/totalizer
Trigger source details	
Analog input (hardware) trigger (CH0 – CH3)	Input signal range: entire span of selected voltage range Channel selectable Trigger level: Programmable (12-bit resolution) Hysteresis: Programmable (12-bit resolution) Latency: 1.25 uS typical Accuracy: ±2% of reading, ±10 mV offset maximum
Analog software trigger (CH0 – CH3)	Trigger range: Anywhere within range of the trigger channel Trigger level: Programmable (16-bit resolution) Latency: one sample period (maximum)
External digital: ▪ (EXT TRIG — BNC or ▪ DIG TRIG — SCSI	Input signal range: –15 V to +15 V maximum Trigger level: TTL level sensitive Minimum pulse width: 50 ns high, 50 ns low Latency: 100ns maximum
Digital pattern triggering DIN0-15	▪ 16-bit pattern triggering on the digital port, DIN0-DIN15 ▪ Programmable for trigger on equal, not equal, above, or below a value. ▪ Individual bits can be masked for "don't care" condition. ▪ Latency: One sample period, maximum
Counter/totalizer triggering: (CTR0-3)	Counter/totalizer inputs (CTR0-3) can trigger an acquisition. User can select to trigger on a frequency or on total counts that are equal, not equal, above, or below a value, or within/outside of a window rising/falling edge. Latency: One sample period, maximum

Pacing sources

Table 12. Pacing specifications

Parameter	Specification
Pacer clocks (2) ▪ Input pacer ▪ Output pacer	Input pacer: ▪ For pacing A/D, DIN and Counter signals ▪ Can be internally generated or externally supplied (XAPCR) ▪ XAPCR is accessible from front BNC or rear SCSI connector Output pacer: ▪ For pacing DAC, DOUT and Timer/PWM signals ▪ Can be internally generated or externally supplied (XDPCR)
Input pacer clock sources (2) ▪ Internal, programmable ▪ External (XAPCR)	Internal, programmable: ▪ Analog channels from 750 ns to 1000s in 20.83 ns steps. ▪ DIN channels and counters from 125 ns* to 100 s in 20.83 ns steps. ▪ Can be configured to pace AO and/or DOUT channels External, TTL level input (XAPCR): ▪ A/D channels down to 750 ns minimum ▪ DIN channels and counters down to 125 ns* minimum ▪ Can be configured to pace DAC and/or DOUT channels
Input pacer rate Internal or external, (XAPCR) source	Analog: 1.33 MHz maximum Digital: 8 MHz if no analog channels are enabled. 1.33 MHz with analog channels enabled.
Pacer input high voltage	2.0 V minimum, 5.5 V maximum
Pacer input low voltage	0.8 V maximum, 0 V minimum
Minimum pulse width	50 ns high, 50 ns low
Output pacer clock sources (4)	▪ Internal output pacer clock, (independent of input pacer clock) ▪ External output pacer clock, XDPCR ▪ Internal input pacing clock ▪ External input pacing clock, XAPCR
Output pacer rate Internal or external, (XDPCR) source	Analog: 1.0 MHz maximum Digital: 8 MHz, if no analog outputs are enabled, (1 MHz if DAC outputs are enabled)
Internal pacer routed to BNC or SCSI conn. ▪ Output high voltage (IOH = –2.5 mA): ▪ Output low voltage (IOL = 2.5 mA):	XAPCR or XDPCR ▪ 2.4 V minimum ▪ 0.4 V maximum

Counters

Table 13. Counter specifications

Parameter	Specification
Number of channels	4 independent CTRL 0,1,2,3 (may be configured as gated if desired)
Modes	Counter, Period, Pulse width, Timing
Counter mode options	Totalize, Clear on Read, Rollover, Stop at top, 16-bit or 32-bit, any other channel can decrement the counter
Period mode options	Measure x1, x10, x100, or x1000 periods, 16-bit or 32-bit, 4 time bases to choose from (20.83 ns, 208.3 ns, 2.083 µs, 20.83 µs), any other channel can gate the period measurement
Pulse width mode options	16-bit or 32-bit values, 4 time bases to choose from (20.83 ns, 208.3 ns, 2.083 µs, 20.83 µs), any other channel can gate the pulse width measurement
Timing mode options	16-bit or 32-bit values, 4 time bases to choose from (20.83 ns, 208.3 ns, 2.083 µs, 20.83 µs)
Resolution	16 or 32-bits
Maximum input frequency	20 MHz
Input type	TTL, rising edge triggered
Absolute maximum input voltage	15V
De-bounce function	16 selections, from 500ns to 25.5ms, pos or neg edge, glitch detect and/or de-bounce modes
Required input current	*±5 µA*
Minimum pulse width	*25 nS high, 25 ns low*
Input high voltage	2.0 V minimum, 5.5 V maximum
Input low voltage	0.8 V maximum, 0 V minimum

Timers

Table 14. Timer specifications

Parameter	Conditions	Specification
Number of channels		Two: TMR/PWM0, TMR/PWM1
Effective frequency range		0.0112 Hz to 24 MHz
Period resolution		20.83 nS
Pulse width resolution		20.83 nS
Output high voltage (IOH = –2.5 mA)		2.4 V minimum
Output low voltage (IOL = 2.5 mA)		0.4 V maximum
Output current		2.5 mA maximum per pin

Quadrature decoders

Table 15. Quadrature decoder specifications

Parameter	Conditions	Specification
Number of decoders		3 (CTR4A, B, Z; CTR5 A, B, Z; CTR6 A, B, Z)
Signals per decoder		A, B and Z
Resolution		16 or 32-bits
Maximum frequency		6 MHz
Minimum pulse width		*25 nS high, 25 ns low*
De-bounce function		16 selections, from 500 ns to 25.5 ms, positive or negative edge, glitch detect, and/or de-bounce modes
Input high voltage		2.0 V minimum, 5.5 V maximum
Input low voltage		0.8 V maximum, 0 V minimum
Absolute maximum input voltage		15 V

Power

Table 16. Power specifications

Parameter	Conditions	Specification
Supply current	Continuous mode	1.5 Amp maximum
+5V EXT output voltage range		4.75 V to 5.25 V
Isolation	Measurement system to PC	500 VDC minimum
AC power adapter specifications (MCC part number PS-5V2AEPS)		
Output voltage		5V, ±5%
Output power		10 watts
Power jack configuration		Two conductor, barrel
Power jack barrel diameter		6.3 mm
Power jack pin diameter		2.0 mm
Power jack polarity		Center positive

USB specifications

Table 17. USB specifications

Parameter	Specification
USB device type	USB 2.0 (high-speed)
USB device compatibility	USB 1.1, 2.0
USB cable length	Three meters maximum.
USB cable type	A-B cable, UL type AWM 2527 or equivalent (minimum 24 AWG VBUS/GND, minimum 28 AWG D+/D-).

Environmental

Table 18. Environmental specifications

Parameter	Specification
Operating temperature range	0 to 55 °C maximum
Storage temperature range	-40 to 85 °C maximum
Humidity	0 to 90% non-condensing

Mechanical

Table 19. Mechanical specifications

Parameter	Specification
Dimensions	142.2 mm W x 180.3 mm D x 38.1 mm H (5.6" x 7.1" x 1.5")
Weight	675 g (1.5 lbs)

I/O cables, connectors and accessories

Table 20. Cables, connectors and accessory specifications

Parameter	Specification
I/O connector type	68-pin standard "SCSI TYPE III" female connector
Compatible cables (for the 68-pin SCSI connector)	▪ CA-68-3R — 68-pin ribbon cable; 3 feet. ▪ CA-68-3S — 68-pin shielded round cable; 3 feet. ▪ CA-68-6S — 68-pin shielded round cable; 6 feet.
Compatible accessory products (for the 68-pin SCSI connector)	▪ TB-102 termination board with screw terminals ▪ RM-TB-100, 19-inch rack mount kit for TB-102

Signal I/O connectors

BNC connectors

Table 21. BNC connectors pin out

BNC signals	Function
CH0	Analog input CH0
CH1	Analog input CH1
CH2	Analog input CH2
CH3	Analog input CH3
EXT TRIG	BNC connection for DIG TRIG*
EXT CLK	BNC connection for XAPCR clock*

*These signals also available at SCSI connector

68-pin SCSI connector

Table 22. 68-pin SCSI connector pin out

Pin No.	Signal	Pin No.	Signal
1	AGND	35	AGND
2	RESERVED	36	RESERVED
3	AGND	37	AGND
4	RESERVED	38	RESERVED
5	AGND	39	AGND
6	VCAL	40	DAC 0
7	+5V PWR	41	DAC 1
8	AGND	42	AGND
9	DIN0	43	DOUT0
10	DIN1	44	DOUT1
11	DIN2	45	DOUT2
12	DIN3	46	DOUT3
13	DIN4	47	DOUT4
14	DIN5	48	DOUT5
15	DIN6	49	DOUT6
16	DIN7	50	DOUT7
17	DIN8	51	DOUT8
18	DIN9	52	DOUT9
19	DIN10	53	DOUT10
20	DIN11	54	DOUT11
21	DIN12	55	DOUT12
22	DIN13	56	DOUT13
23	DIN14	57	DOUT14
24	DIN15	58	DOUT15
25	CTR4 A	59	CTR0
26	CTR4 B	60	CTR1
27	CTR4 Z	61	CTR2
28	CTR5 A	62	CTR3
29	CTR5 B	63	TMR/PWM0
30	CTR5 Z	64	TMR/PWM1
31	CTR6 A	65	DIG TRIG
32	CTR6 B	66	XAPCR
33	CTR6 Z	67	XDPCR
34	DGND	68	DGND

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